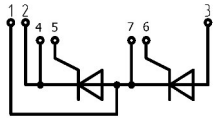
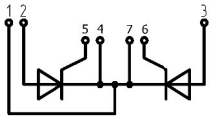
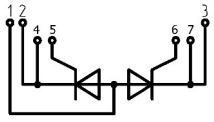
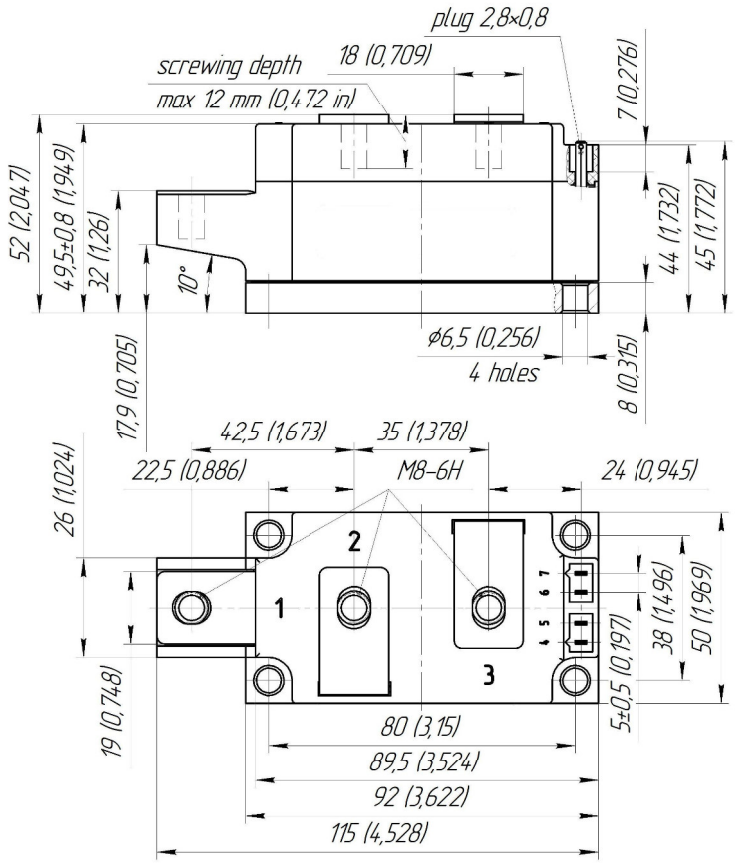
Electrically isolated base plate
Industrial standard package
Simplified mechanical design, rapid assembly
Pressure contact

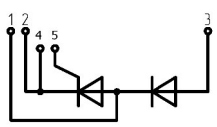
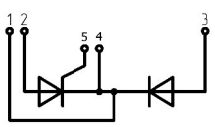
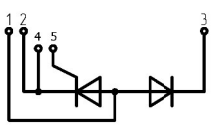
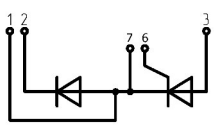
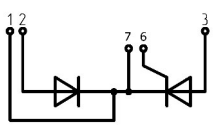
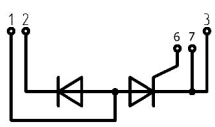
Double Thyristor Module For Phase Control MTx-320-18-C1

Mean on-state current				I_{TAV}		320 A		
Repetitive peak off-state voltage				V_{DRM}		1000 ÷ 1800 V		
Repetitive peak reverse voltage				V_{RRM}				
Turn-off time				t_q		160 µs		
V_{DRM}, V_{RRM}, V	1000	1100	1200	1300	1400	1500	1600	1800
Voltage code	10	11	12	13	14	15	16	18
T_j, °C	– 40 ÷ 130							

MT3 **MT4** **MT5**



MT/D3 **MT/D4** **MT/D5** **MD/T3** **MD/T4** **MD/T5**

All dimensions in millimeters (inches)

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Mean on-state current	A	320 348	T_c=90 °C; T_c=85 °C; 180° half-sine wave; 50 Hz	
I_{TRMS}	RMS on-state current	A	502	T_c=90 °C; 180° half-sine wave; 50 Hz	
I_{TSM}	Surge on-state current	kA	8.5 10.0	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=10 ms; single pulse; V_D=V_R=0 V; Gate pulse:I_G=2 A; t_{GP}=50 μs; di_G/dt≥1 A/μs
			9.0 10.5	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=8.3 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 μs; di_G/dt≥1 A/μs
I^2t	Safety factor	$A^2s{\cdot}10^3$	360 500	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=10 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 μs; di_G/dt≥1 A/μs
			330 450	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=8.3 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 μs; di_G/dt≥1 A/μs
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	1000÷1800	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; 50 Hz; Gate open	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	1100÷1900	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; single pulse; Gate open	
V_D, V_R	Direct off-state and Direct reverse voltages	V	$0.75{\cdot}V_{DRM}$ $0.75{\cdot}V_{RRM}$	T_j=$T_{j\,max}$; Gate open	
TRIGGERING					
I_{FGM}	Peak forward gate current	A	6	T_j=$T_{j\,max}$	
V_{RGM}	Peak reverse gate voltage	V	5		
P_G	Gate power dissipation	W	3	T_j=$T_{j\,max}$ for DC gate current	
SWITCHING					
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/μs	200	T_j=$T_{j\,max}$; V_D=$0.67{\cdot}V_{DRM}$; I_{TM}=2 I_{TAV}; Gate pulse: I_G=2 A; t_{GP}=50 μs; di_G/dt≥2 A/μs	
THERMAL					
T_{stg}	Storage temperature	°C	- 40 ÷ 50		
T_j	Operating junction temperature	°C	- 40 ÷ 130		
$T_{c\,op}$	Operating temperature	°C	- 40 ÷ 130		
MECHANICAL					
a	Acceleration under vibration	m/s^2	50		

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	1.40	T_j=25 °C; I_{TM}= 785 A	
$V_{T(TO)}$	On-state threshold voltage, max	V	0.75	T_j=$T_{j\,max}$;	
r_T	On-state slope resistance, max	mΩ	0.500	0.5 π I_{TAV} < I_T < 1.5 π I_{TAV}	
I_L	Latching current, max	mA	700	T_j=25 °C; V_D=12 V; Gate pulse: I_G=2 A; t_{GP}=50 μs; di_G/dt≥1 A/μs	
I_H	Holding current, max	mA	300	T_j=25 °C; V_D=12 V; Gate open	
BLOCKING					
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	40	T_j=$T_{j\,max}$; V_D=V_{DRM}; V_R=V_{RRM}	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage, min	V/μs	1000	T_j=$T_{j\,max}$; V_D=0.67·V_{DRM}; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	3.50 2.00 1.50	T_j= $T_{j\,min}$ T_j=25 °C T_j= $T_{j\,max}$	V_D=12 V; I_D=3 A; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	250 150 100	T_j= $T_{j\,min}$ T_j= 25 °C T_j= $T_{j\,max}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.25	T_j=$T_{j\,max}$; V_D=0.67·V_{DRM}; Direct gate current	
I_{GD}	Gate non-trigger direct current, min	mA	10.00		
SWITCHING					
t_{gd}	Delay time	μs	2.00	T_j=25 °C; V_D=0.4·V_{DRM}; I_{TM}=I_{TAV}; Gate pulse: I_G=2 A; t_{GP}=50 μs; di_G/dt≥2 A/μs	
t_q	Turn-off time, max	μs	160	dv_D/dt=50 V/μs; T_j=$T_{j\,max}$; I_{TM}=325 A; di_R/dt=-10 A/μs; V_R=100V; V_D=0.67 V_{DRM}	
Q_{rr}	Total recovered charge, max	μC	820	T_j=$T_{j\,max}$; I_{TM}=500 A; di_R/dt=-10 A/μs; V_R=100 V	
t_{rr}	Reverse recovery time, max	μs	15		
I_{rrM}	Peak reverse recovery current, max	A	110		
THERMAL					
R_{thjc}	Thermal resistance, junction to case			180° half-sine wave, 50 Hz	
	per module	°C/W	0.0550		
	per arm	°C/W	0.1100		
R_{thch}	Thermal resistance, case to heatsink				
	per module	°C/W	0.0200		
	per arm	°C/W	0.0400		
INSULATION					
V_{ISOL}	Insulation test voltage	kV	3.00	Sine wave, 50 Hz; RMS	t=1 min
			3.60		t=1 sec
MECHANICAL					
M_1	Mounting torque (M6)[1)]	Nm	6.00	Tolerance ± 15%	
M_2	Terminal connection torque (M8)[1)]	Nm	9.00	Tolerance ± 15%	
w	Weight	g	800		

PART NUMBERING GUIDE	NOTES
MT 3 - 320 - 18 - C1 - N 1 2 3 4 5 6 1. Thyristor module (MT) Thyristor – Diode module (MT/D) Diode – Thyristor module (MD/T) 2. Circuit Schematic 3. Average On-state Current, A 4. Voltage Code 5. Package Type (M.C1) 6. Ambient Conditions: N – Normal	[1)] The screws must be lubricated

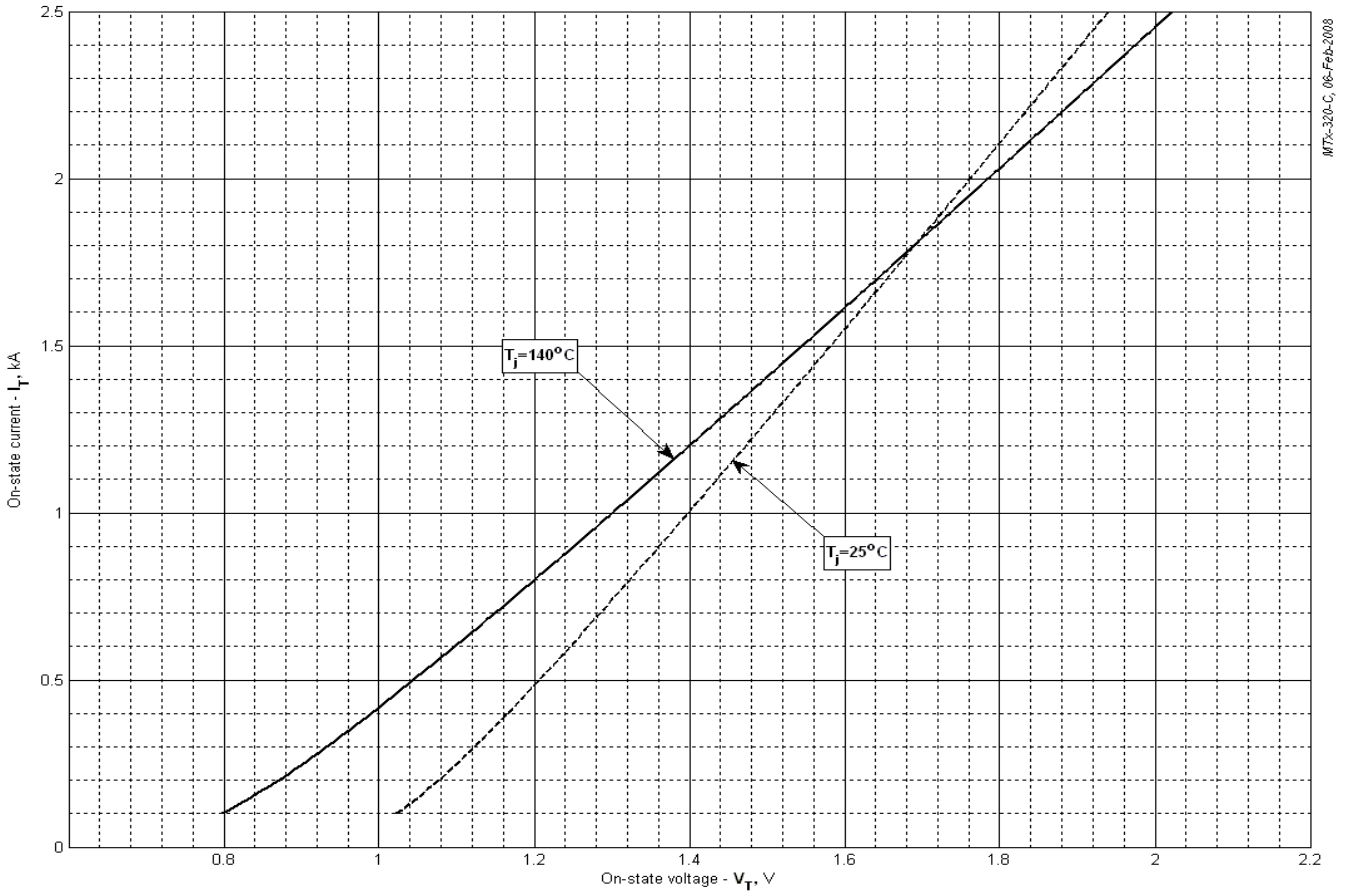


Fig 1 – On-state characteristics of Limit device

Analytical function for On-state characteristic:

$$V_T = A + B \cdot i_T + C \cdot \ln(i_T + 1) + D \cdot \sqrt{i_T}$$

	Coefficients for max curves	
	T_j = 25°C	T_j = $T_{j\,max}$
A	0.920852	0.658423
B	0.313282	0.414813
C	-0.152242	-0.210993
D	0.269777	0.373886

On-state characteristic model (see Fig. 1)

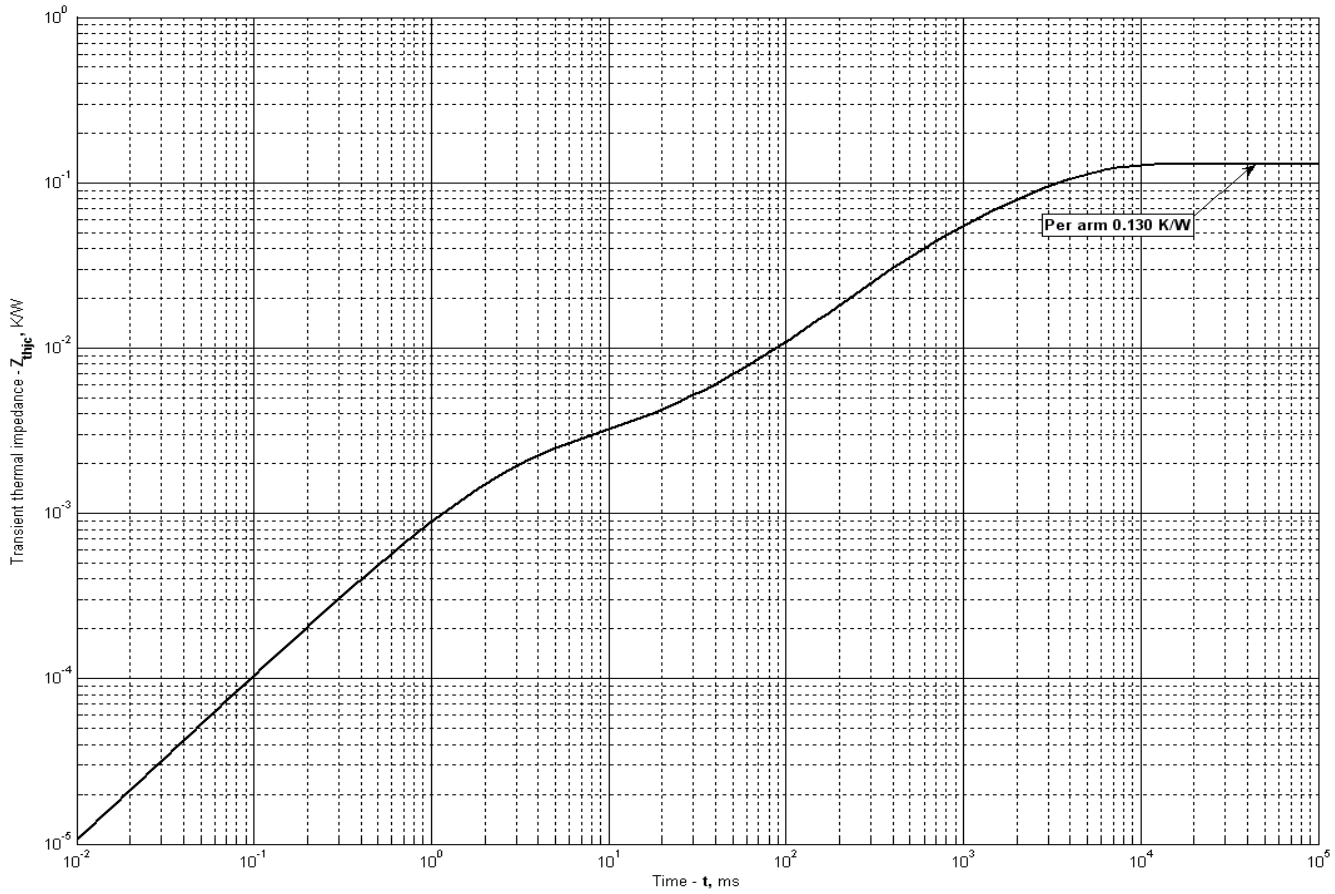


Fig 2 – Transient thermal impedance

Analytical function for Transient thermal impedance junction to case Z_{thjc} for DC:

$$Z_{thjc} = \sum_{i=1}^{n} R_i \left(1 - e^{-\frac{t}{\tau_i}} \right)$$

Where ***i*** = 1 to ***n***, ***n*** is the number of terms in the series.

t = Duration of heating pulse in seconds.

$\mathbf{Z_{thjc}}$ = Thermal resistance at time t.

$\mathbf{R_i}$ = Amplitude of p_{th} term.

$\mathbf{t_i}$ = Time constatnt of r_{th} term.

i	1	2	3	4	5	6
$\mathbf{R_i}$, **K/W**	0.1008	0.007806	0.02226	-0.007688	0.004709	0.002168
τ_i, **s**	2.801	1.283	0.3281	0.09408	0.0572	0.002255

Transient thermal impedance junction to case Z_{thjc} model (see Fig. 2)

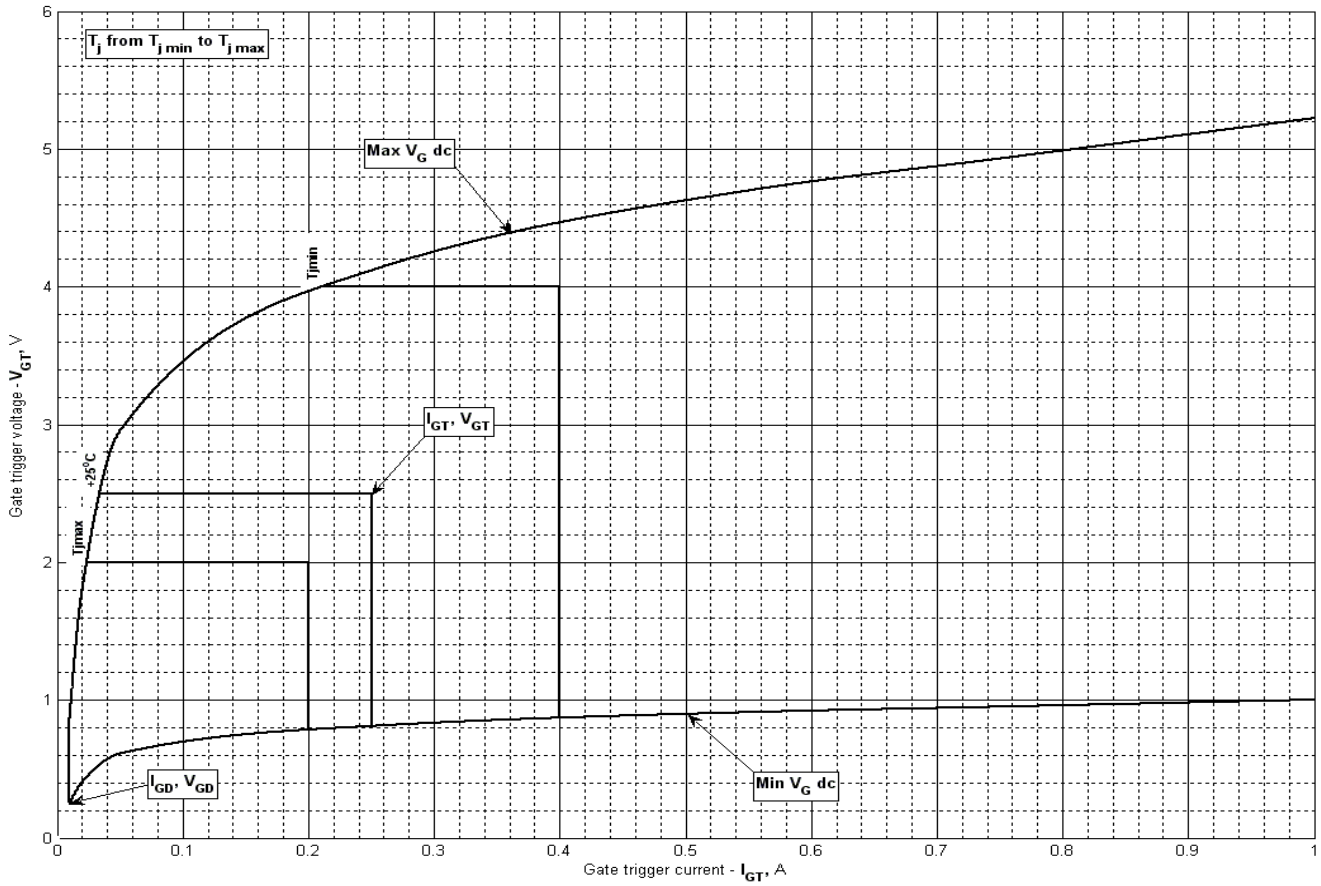


Fig 3 – Gate characteristics – Trigger limits

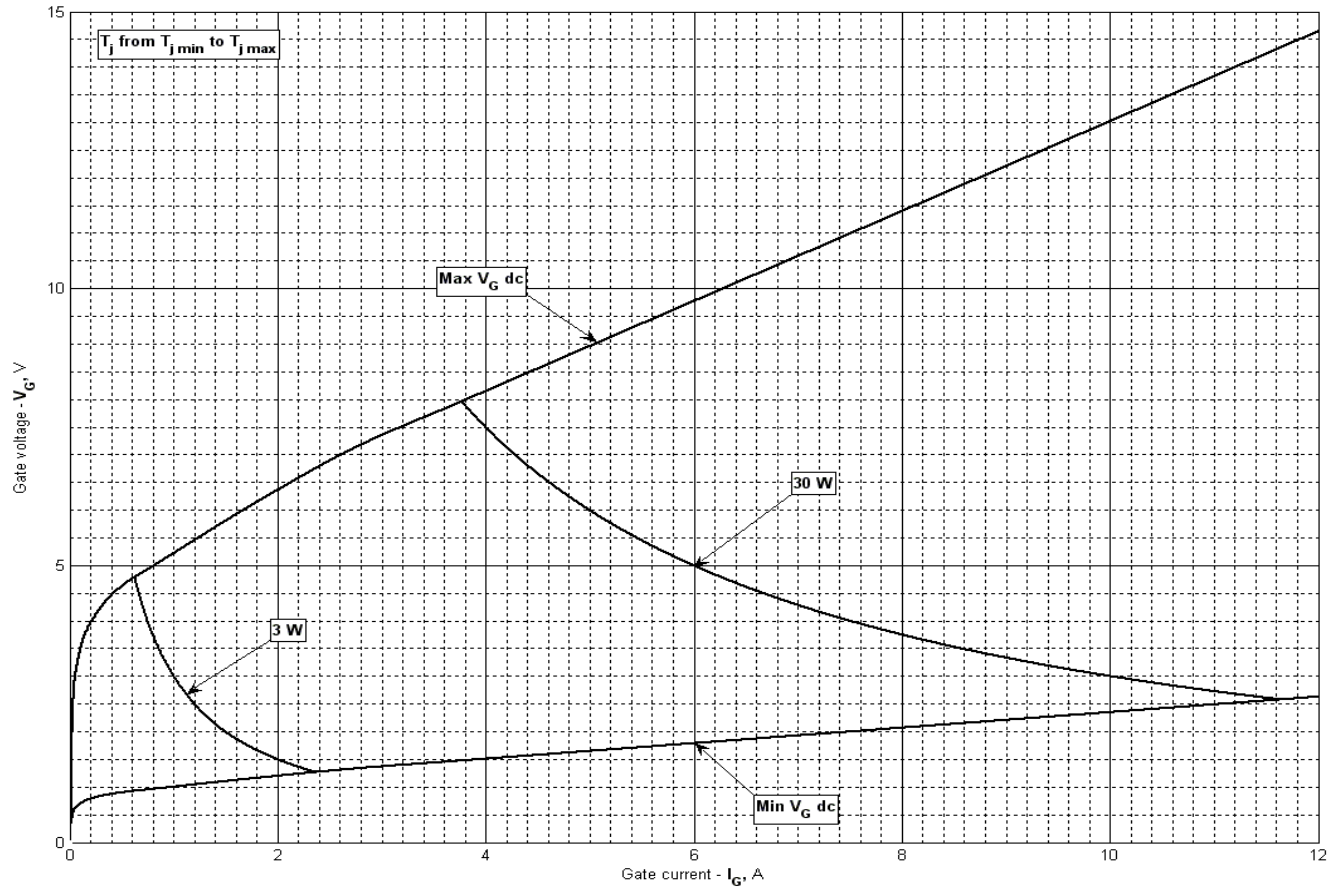


Fig 4 - Gate characteristics – Power curves

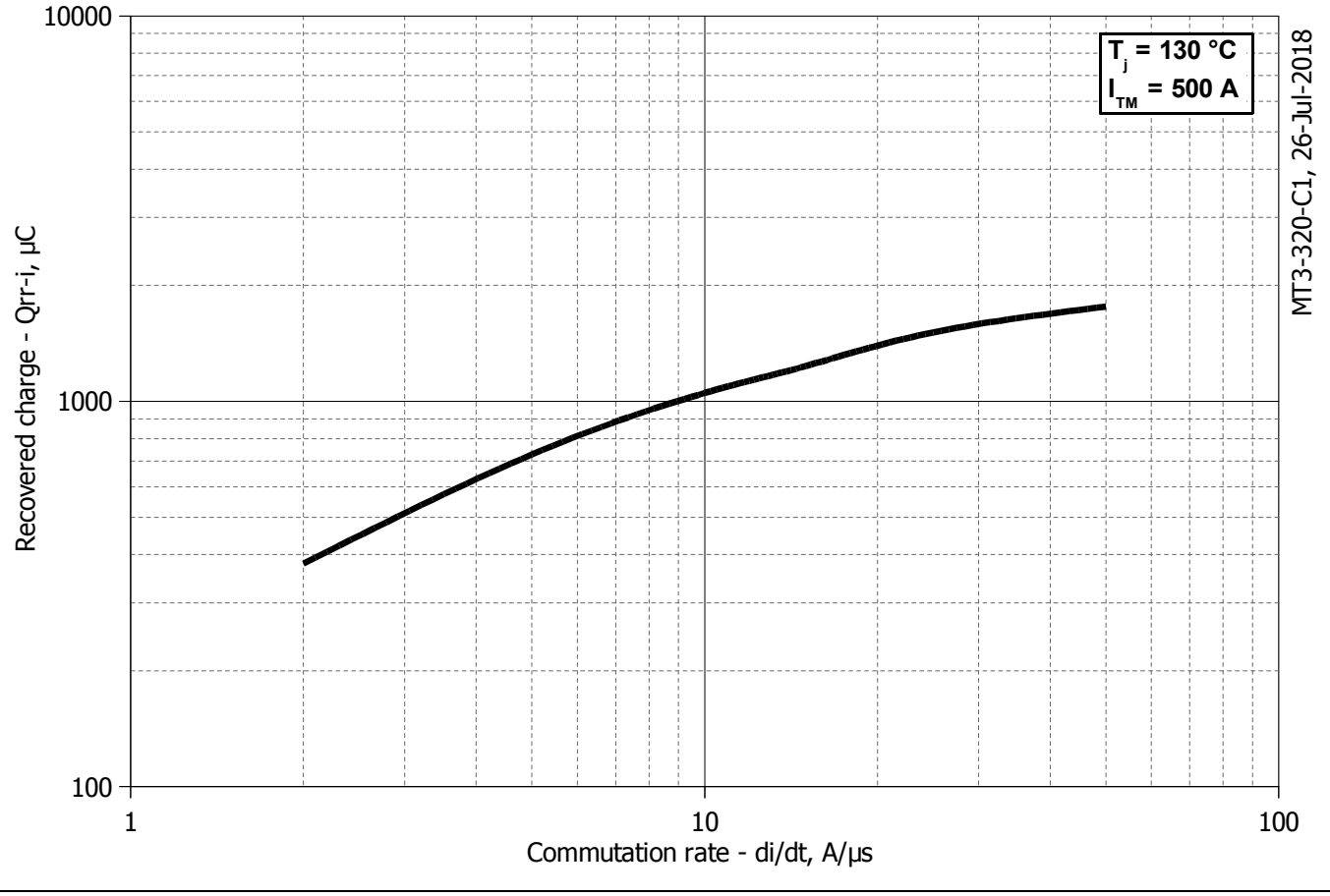


Fig 5 - Total recovered charge, Q_{rr-i} (integral)

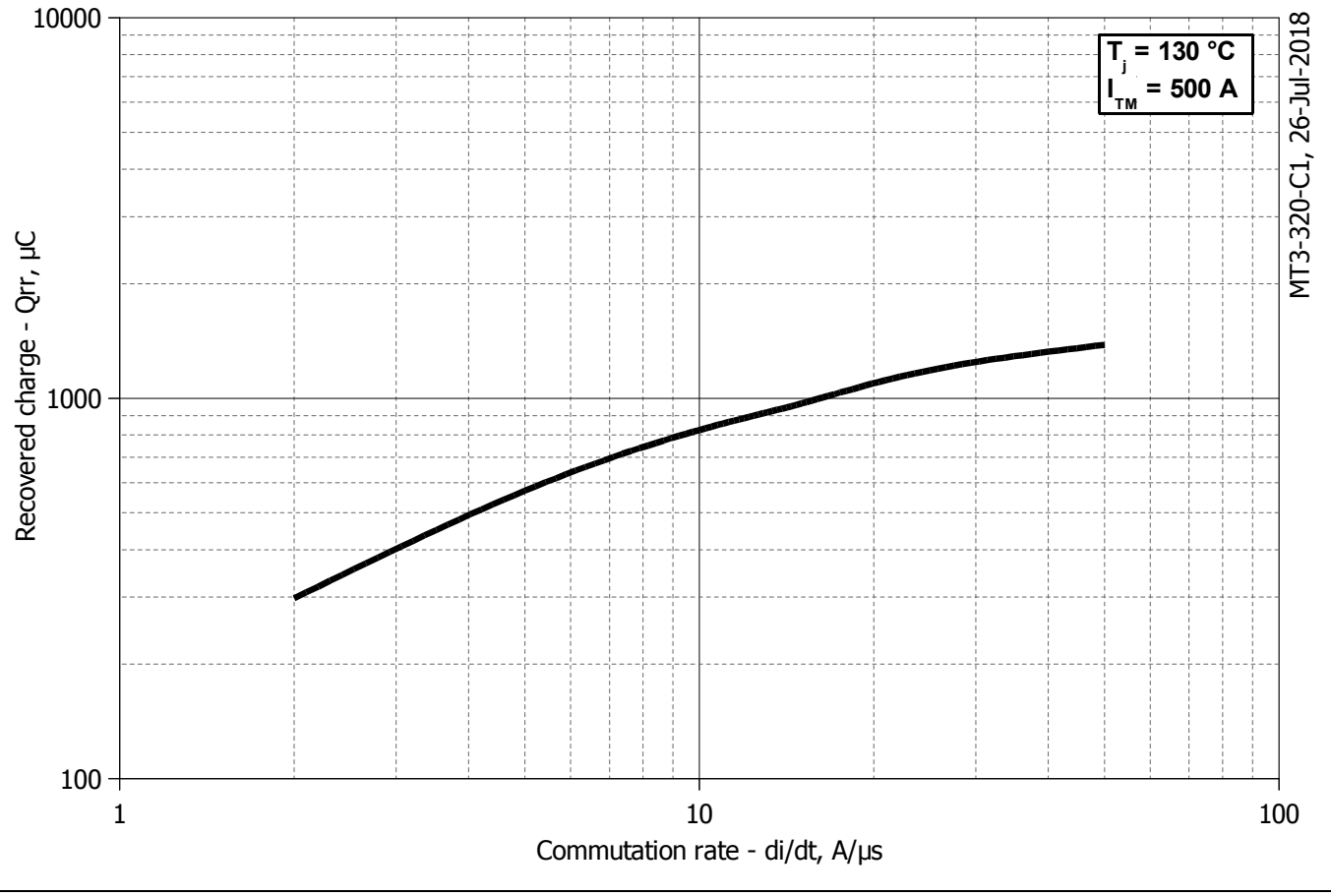


Fig 6 - Recovered charge, Q_{rr} (25% chord)

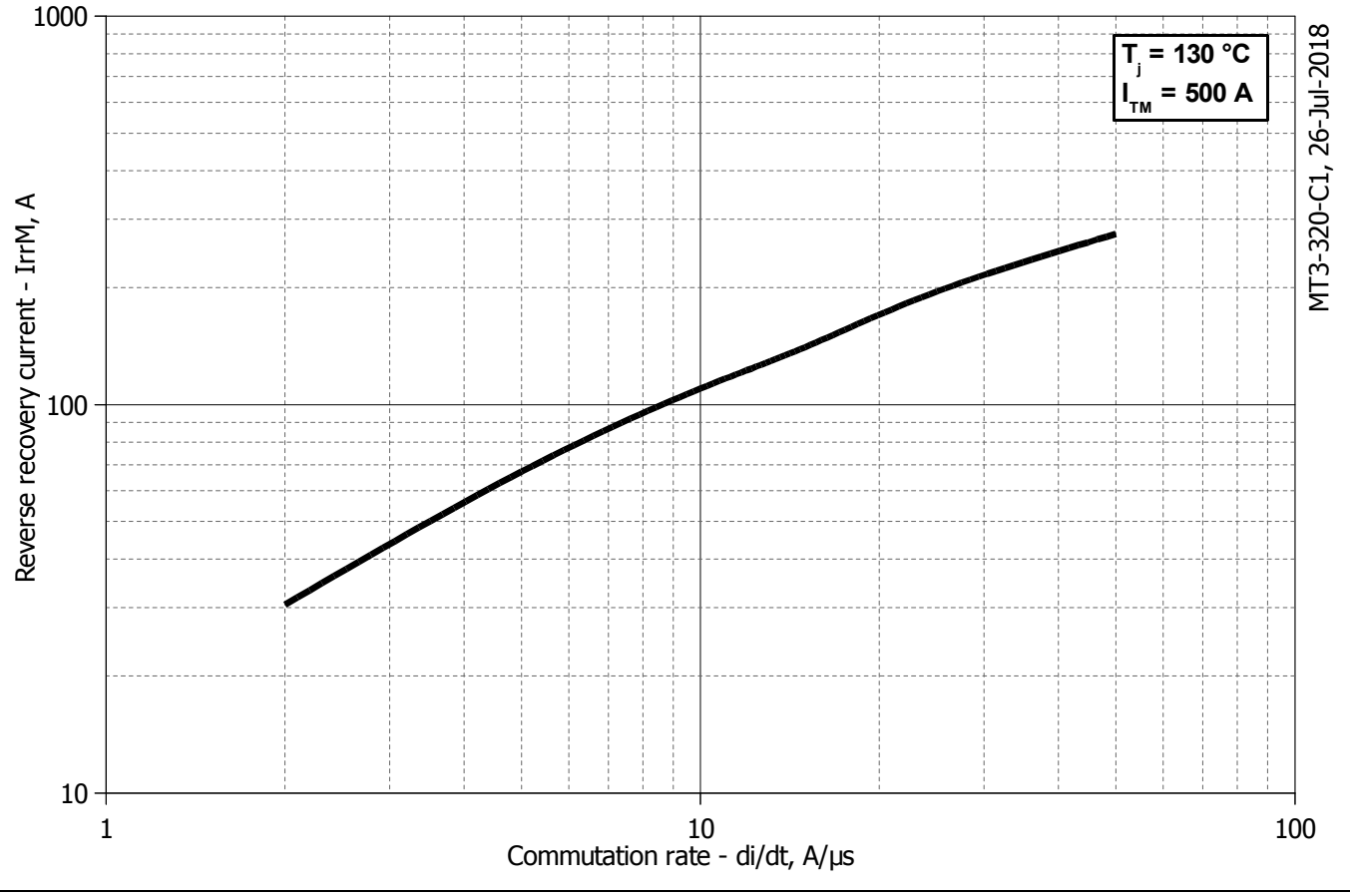


Fig 7 - Peak reverse recovery current, I_{rrM}

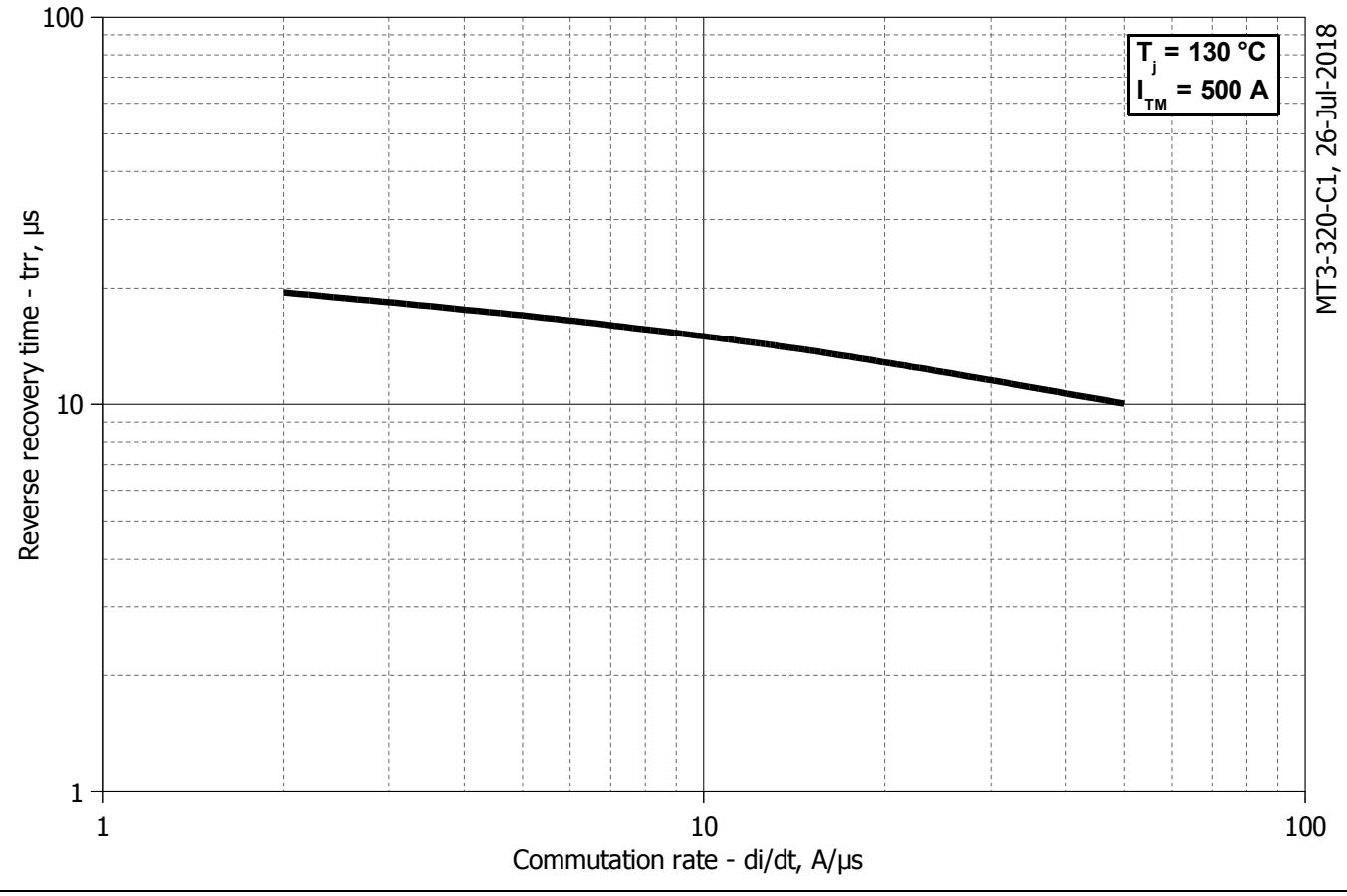


Fig 8 - Maximum recovery time, t_{rr} (25% chord)

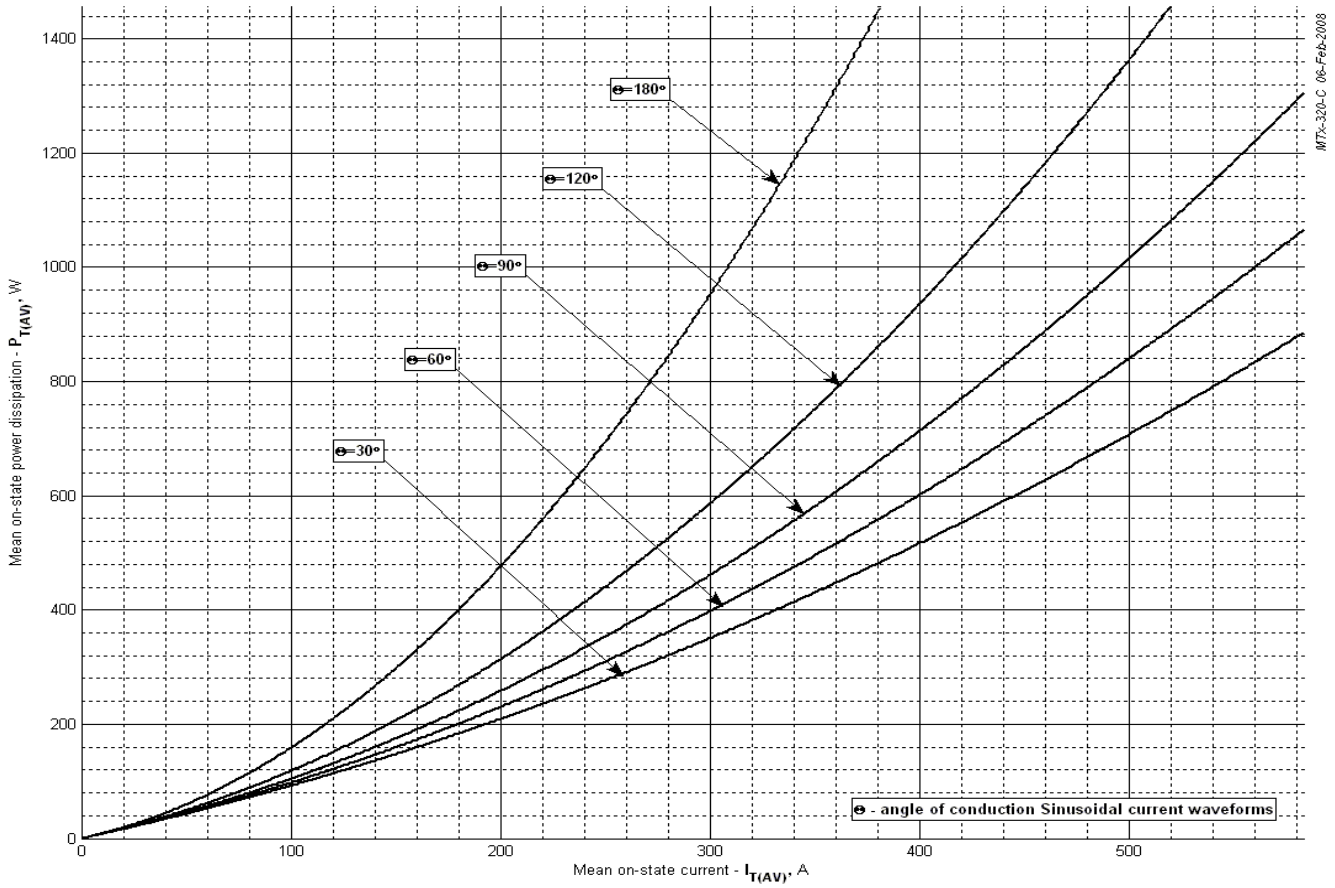


Fig 9 – On-state power loss (sinusoidal current waveforms)

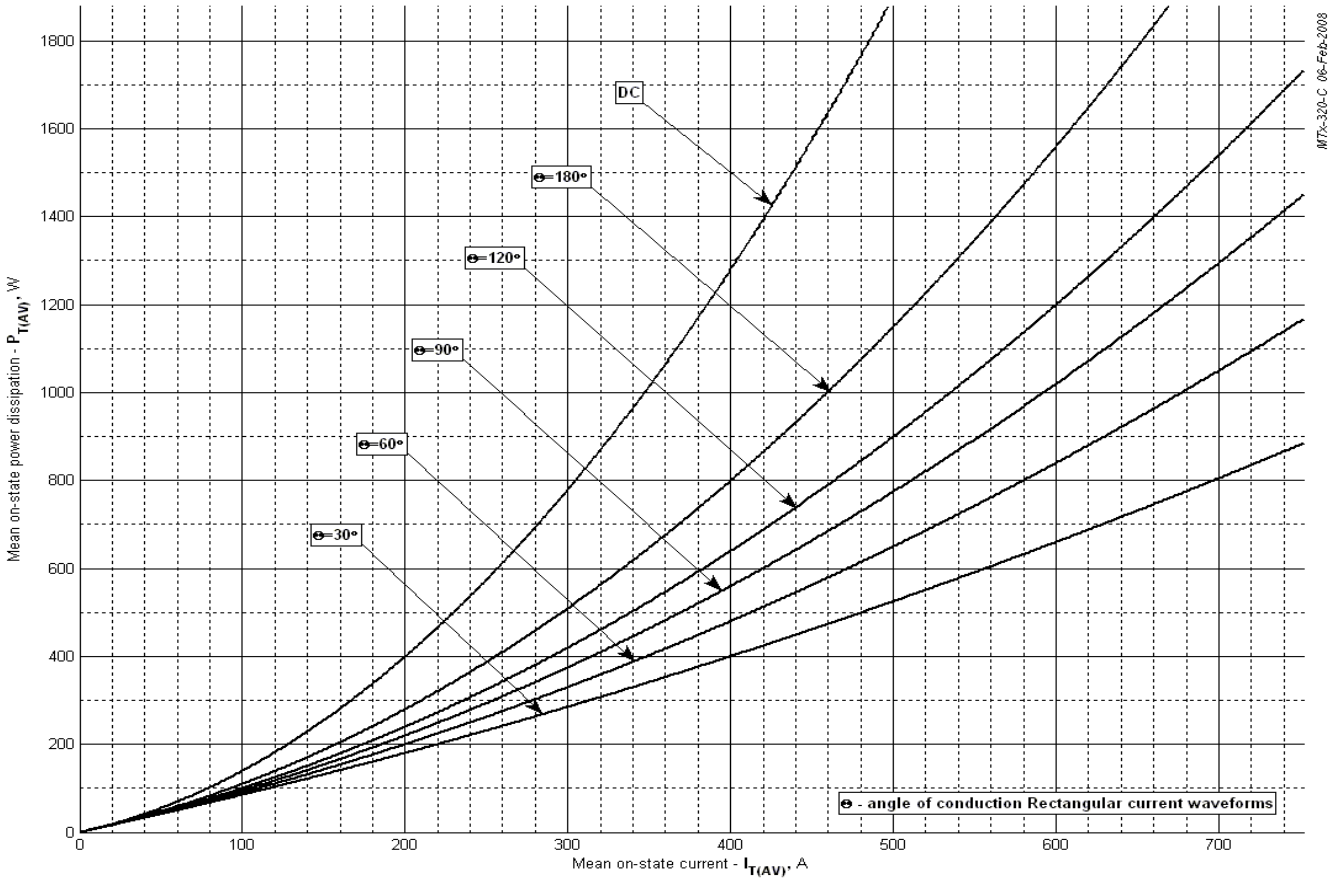


Fig 10 - On-state power loss (rectangular current waveforms)

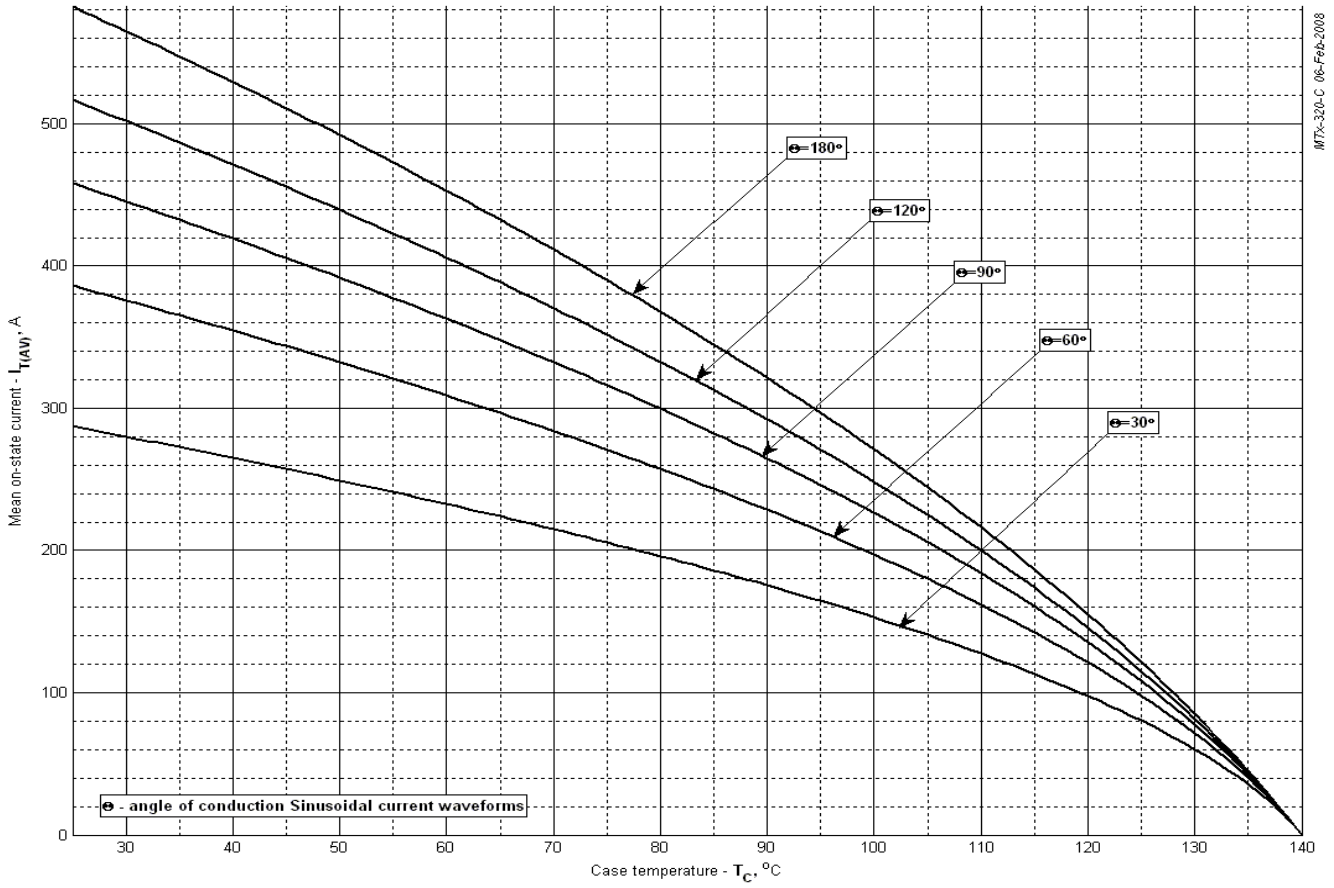


Fig 11 – Maximum case temperature (sinusoidal current waveforms)

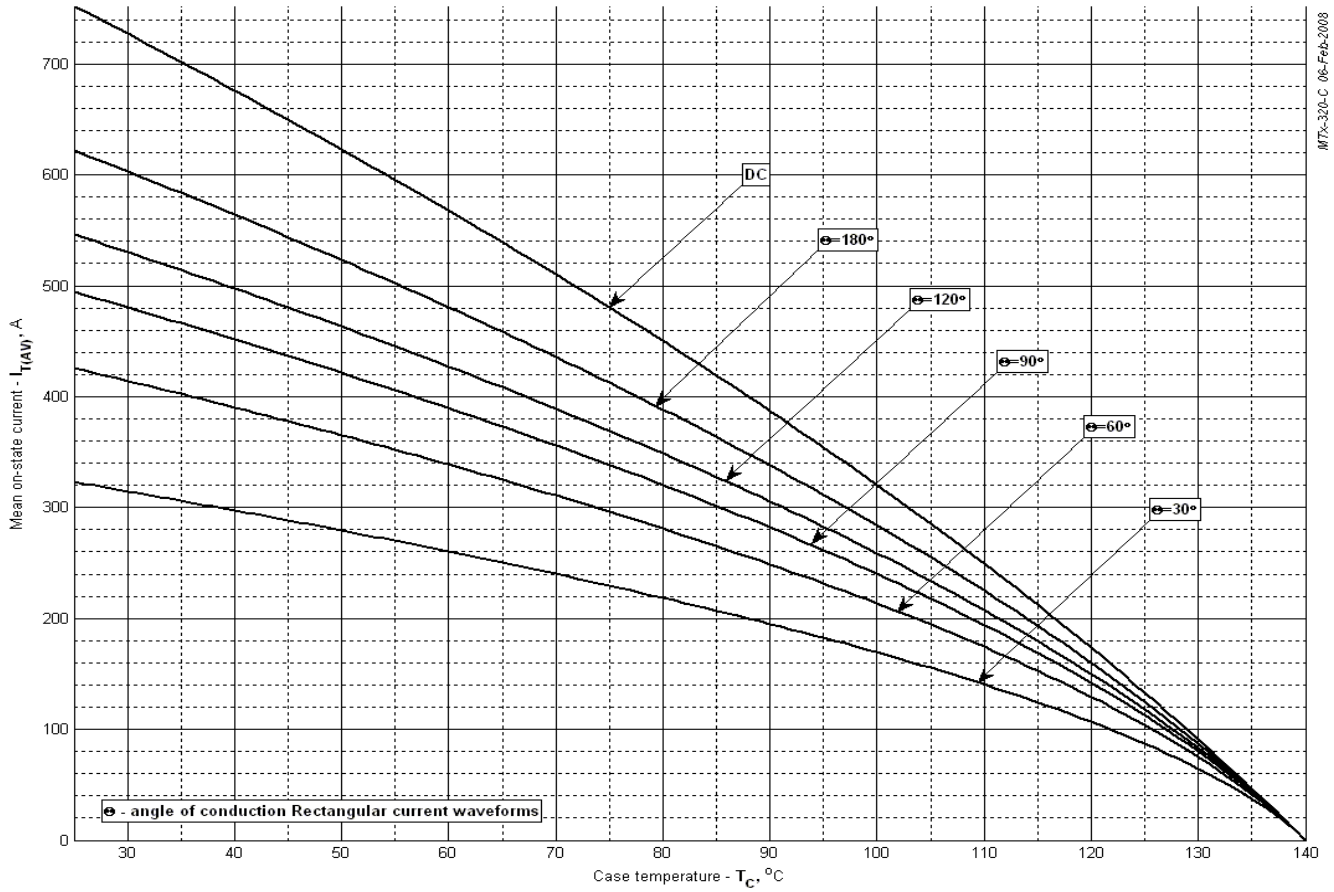


Fig 12 - Maximum case temperature (rectangular current waveforms)

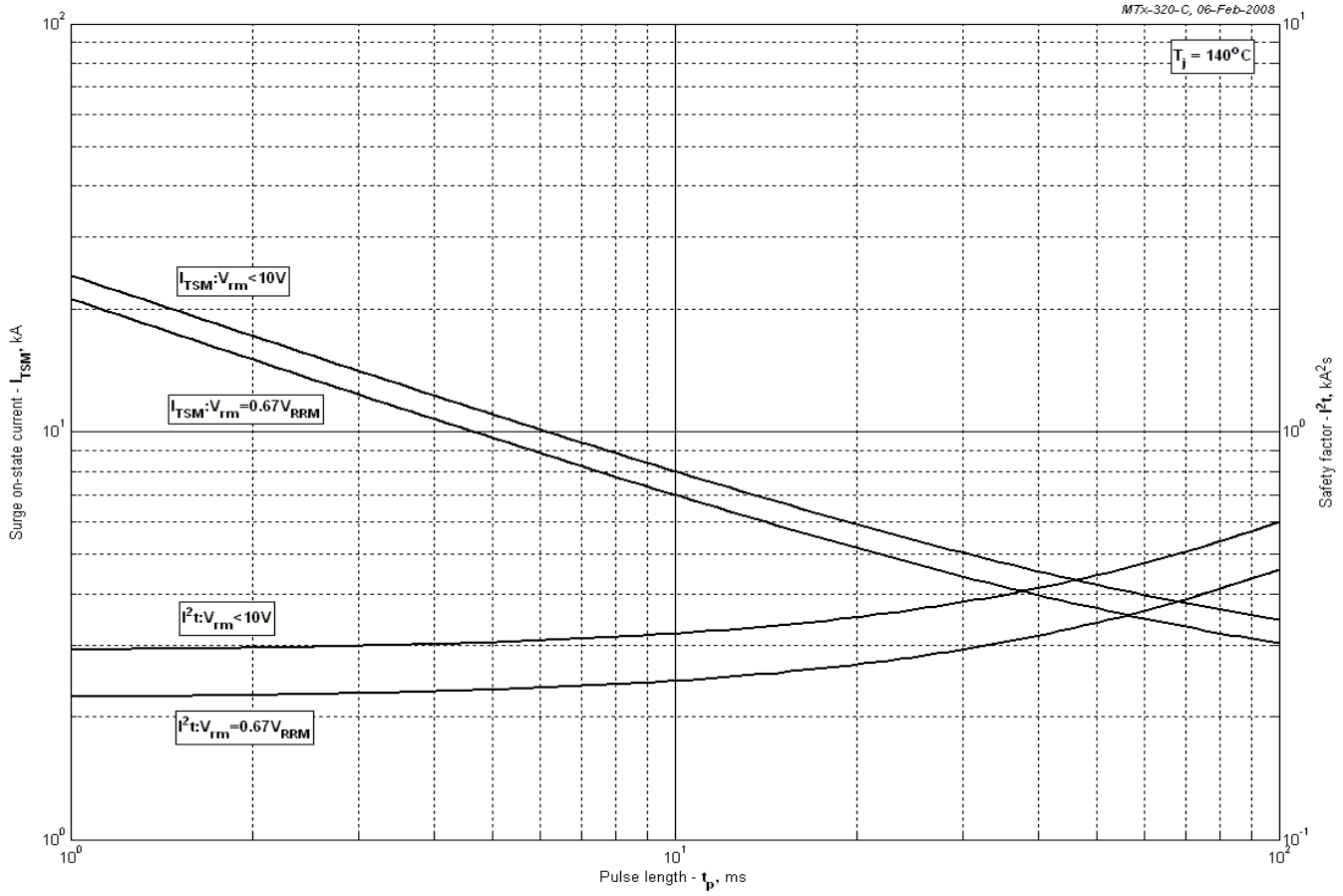


Fig 13 – Maximum surge and I^2t ratings

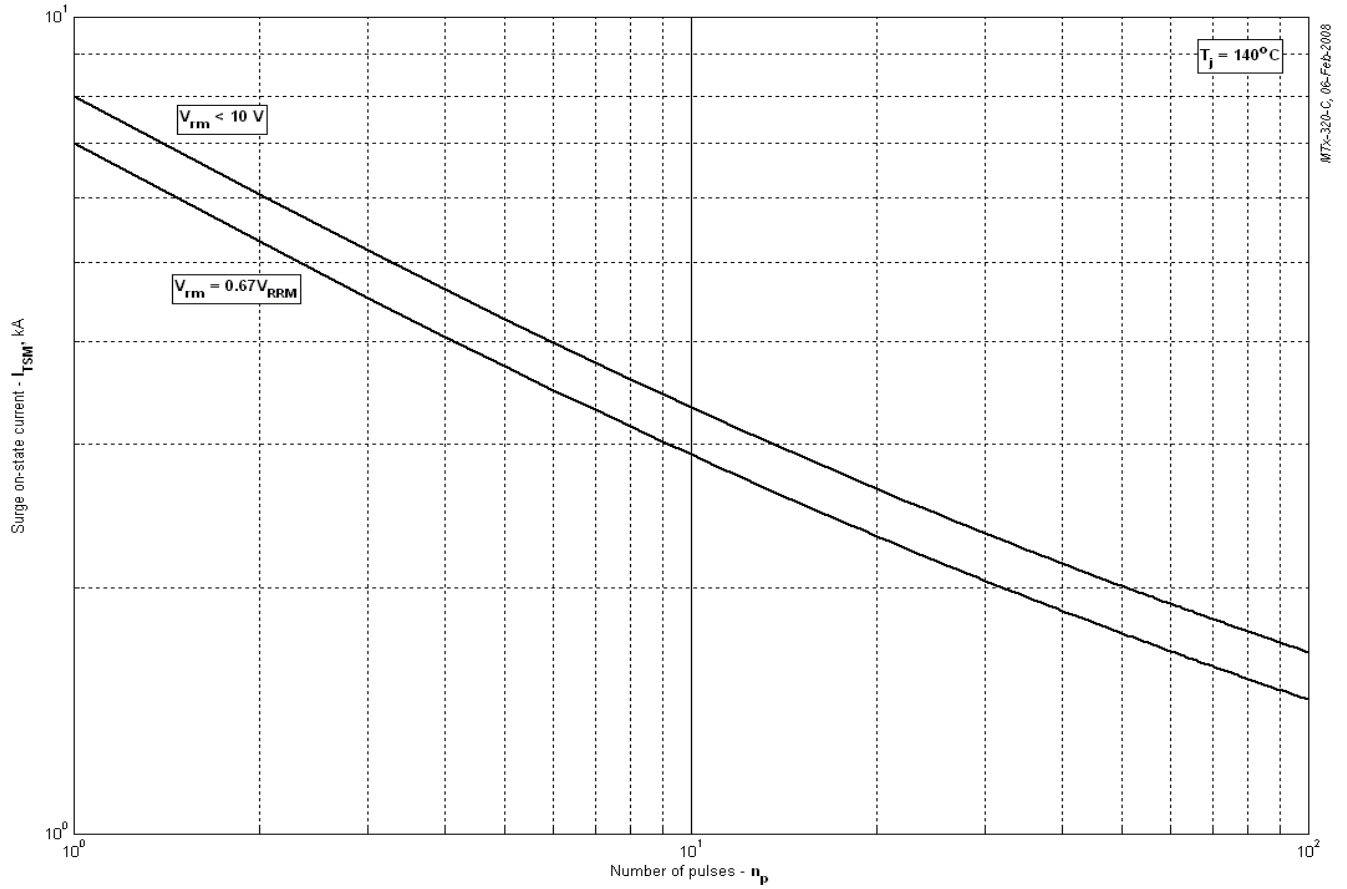


Fig 14 - Maximum surge ratings